REMARKS/ARGUMENTS

Rejections under 35 U.S.C. § 102(b)

In the Office Action mailed May 4, 2005, claims 1-17 and 21-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,953,249 to Jan P. van der Wagt (herein "*van der Wagt*"). Applicants respectfully request reconsideration of this rejection for at least the following reasons.

As for claim 1, claim 1 as amended recites:

> A two-transistor DRAM cell comprising:
> an NMOS device with a gate;
> a PMOS device with a gate, the PMOS device coupled to the NMOS device; and
> a storage node coupled to the second gate.
> [underline added]

In rejecting claim 1, the Examiner cites *van der Wagt*, which discloses two-transistor DRAM cells that include p-channel and n-channel FETs. However, each of the two-transistor DRAM cells that are taught in *van der Wagt* have the p-channel FET as the write device, while the n-channel FET as the read device. *See* figures 2a to 2d, and figure 4 of *van der Wagt*. *Van der Wagt* does not disclose or suggest a two-transistor DRAM cell that includes an NMOS as the write device, and a PMOS as the read device, wherein the storage node is coupled to the gate of the PMOS. For at least these reasons, claim 1 is patentable over *van der Wagt*. Amended independent claim 21 has features similar to those in amended independent claim 1. Therefore, for at least the same reasons that claim 1 is patentable over *van der Wagt*, claim 21 is also patentable over *van der Wagt*.

As for independent claim 11, the Examiner in rejecting claim 11 states that

> Van der Wagt discloses a DRAM cell (Figure 4) comprising:
> a read bit line (BL);
> a write bit line (BL);
> a read word line (READ WL);
> a write word line (WRITE WL);
> an n-channel (NMOS) device (22) coupled between the read bit line and the read word line; and

a p-channel (PMOS) device (20) coupled to the NMOS device so as to define a storage node (SN) therebetween.

* See page 3 of the Office Action, underline added.

Applicants respectfully submit that claim 11 does not recite such features. In particular, claim 11 does not recite "*an n-channel (NMOS) device (22)* coupled between the read bit line and the read word line; and *a p-channel (PMOS) device (20)* coupled to the NMOS device so as to define a storage node (SN) therebetween." Instead, claim 11 recites, among other things, "*a p-channel (PMOS) device* coupled between the read bit line and the read word line; and *an n-channel (NMOS) device* coupled between the write bit line and a gate region of the PMOS device so as to form a storage node therebetween." The DRAM cells as taught in *van der Wagt* are not configured in such manner. For at least these reasons, claim 11 is patentable over *van der Wagt*.

Claims 2, 3, 12-17, 22, and 23 depend from and add additional features to independent claims 1, 11, and 21. Therefore, by virtue of their dependency, claims 2, 3, 12-17, 22, and 23 are also patentable over *van der Wagt*.

CONCLUSION

In view of the foregoing, the Applicants respectfully submit that claims 1-3, 11-17 and 21-23 are in condition for allowance. Thus, early issuance of Notice of Allowance is respectfully requested.

If the Examiner has any questions, he is invited to contact the undersigned at (503) 796-2099.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393.

Respectfully submitted,
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